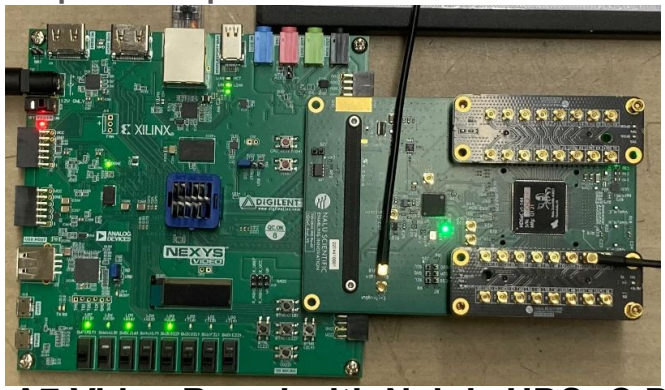
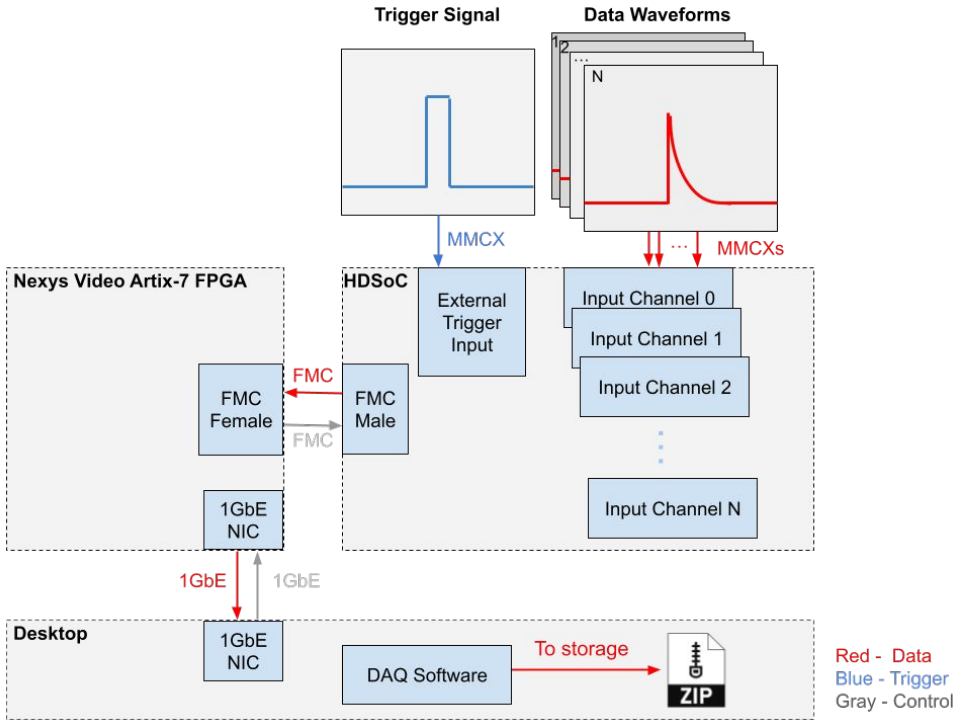
ATAR DAQ - Hardware

- DAQ is functional and integrated into MIDAS
- Can digitize data rates up to 55 MB/s, event rates up to 30 kHz*

*For specific parameters



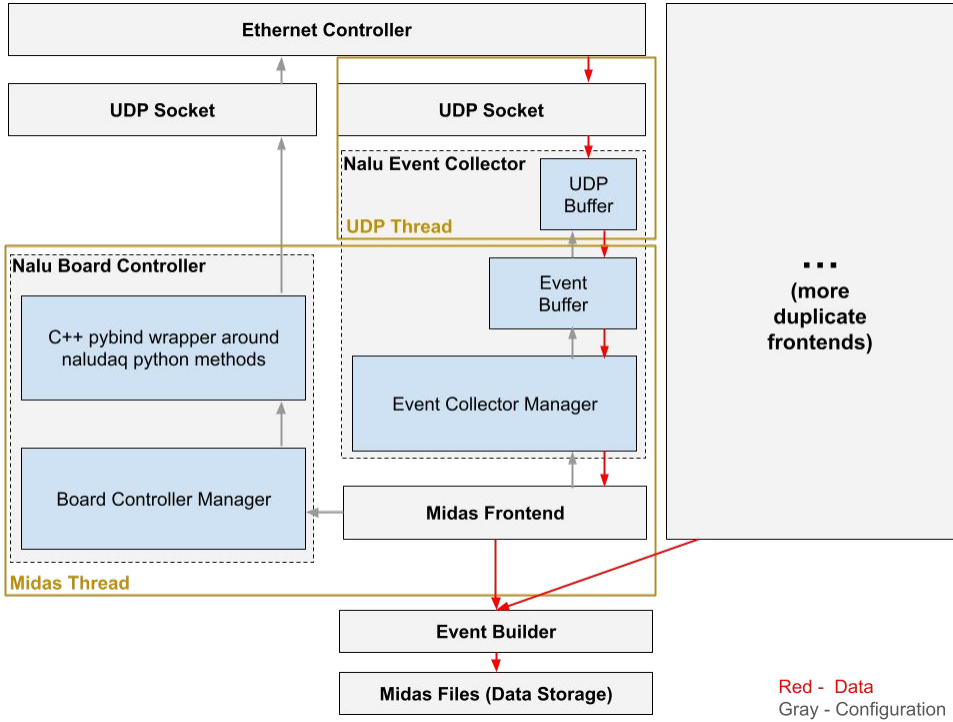
Nexys A7 Video Board with Nalu's HDSoC Digitizer Attached as an FMC Module



Conceptual Hardware Diagram for the HDSoC Readout

ATAR DAQ - Software

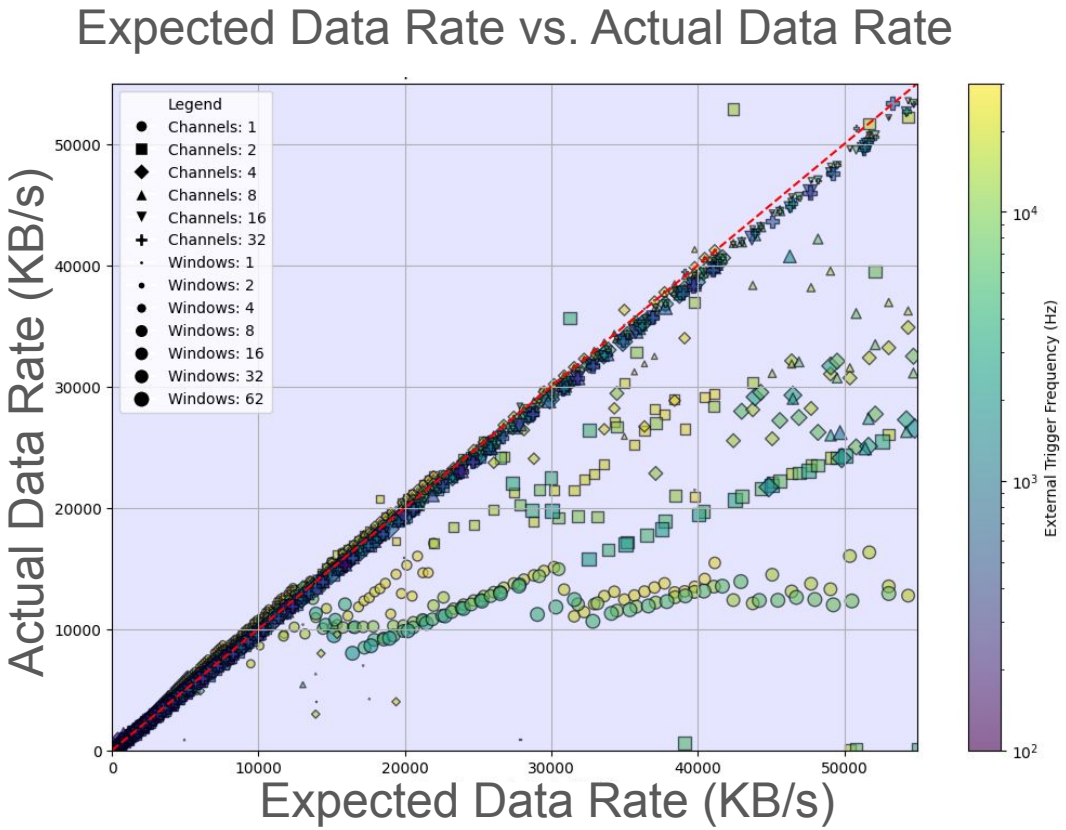
- Wrote a midas frontend that leverages custom libraries created for readout
  - Nalu Board Controller
  - Nalu Event Collector
- Separate branch for rate testing, leveraging custom RP Pico W libraries created for automatic rate testing
  - RP Pico W remote controller
  - RP Pico W board interface



Conceptual Software Diagram for the HDSoC Readout

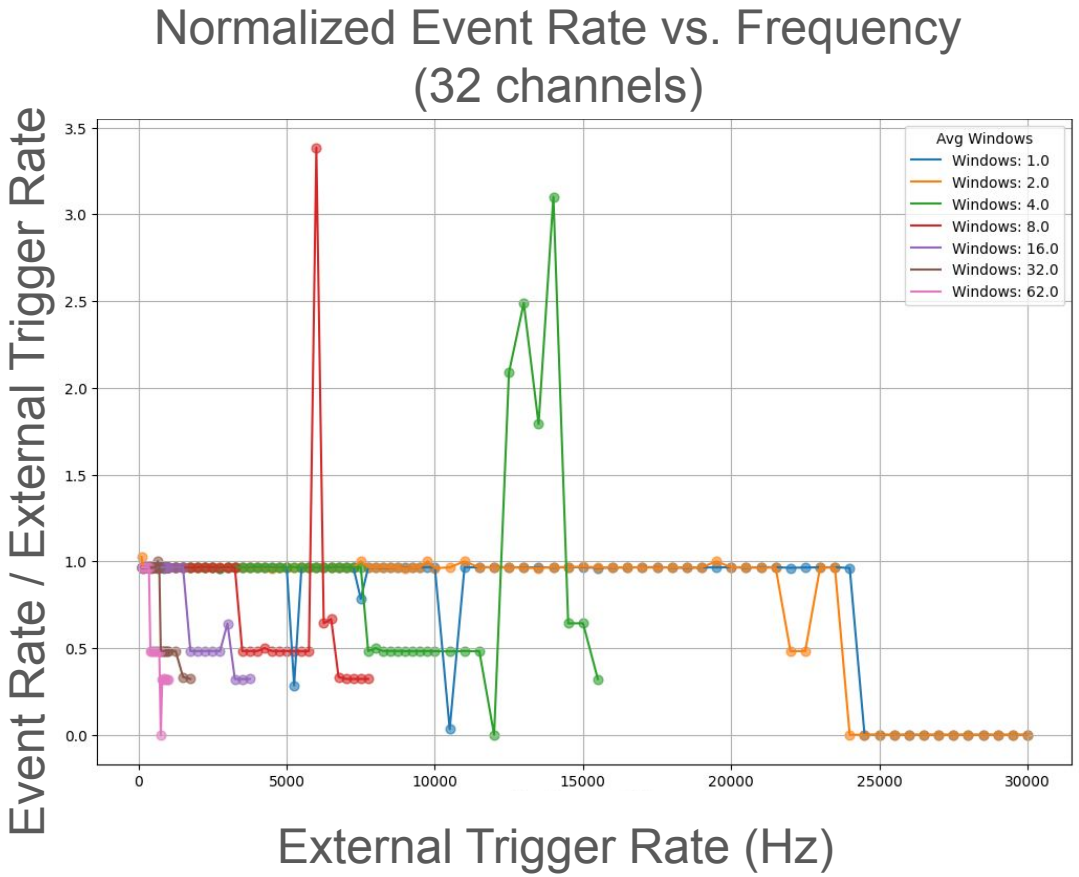
ATAR DAQ - Rate Tests

- Majority of input parameters → performance as expected
- Outliers where we underperform
  - Expect good performance under 55 MB/s
  - Looking for cause of performance drops



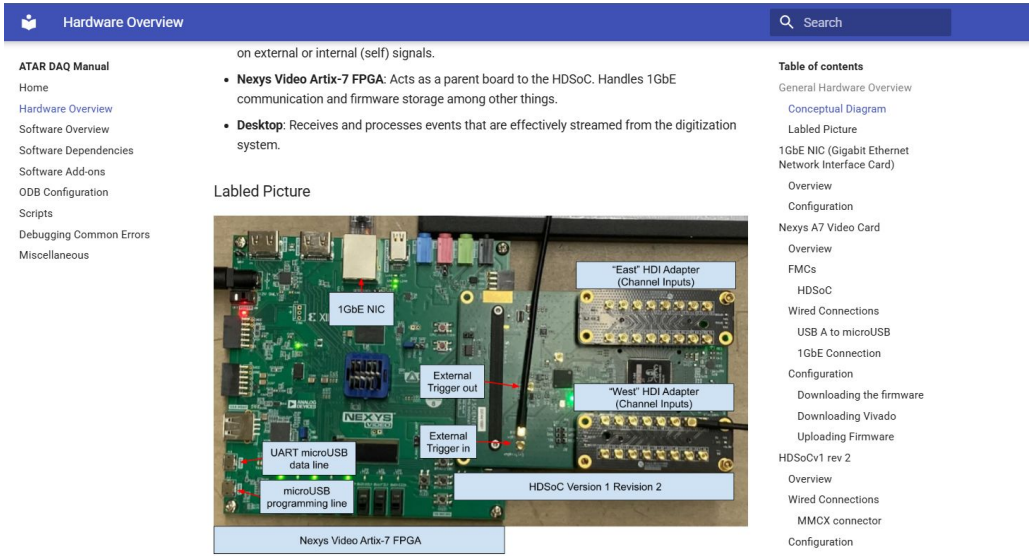
ATAR DAQ - Rate Tests

- For 32 channels (all active)
- 1 window = 32 12-bit ADC samples
- 1 Gsps
- Can take 32 traces length 64 ns at rates ~20kHz reliably
- Events begin dropping near 55 MB/s threshold
- Need to test self/internal triggering mode still
    - In these plots every channel is digitized on every trigger



ATAR DAQ - Useful Documents

- ATAR DAQ manual hosted on github pages
  - Hardware setup guides
  - Software setup guides
  - ODB configuration and usage
  - Etc.
- More rate testing plots available
  - See my notes page
- Documentation and examples available in project README.md files



A screenshot of a page on the ATAR DAQ Manual